

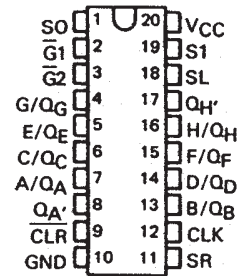
# SN54LS299, SN54S299, SN74LS299, SN74S299 8-BIT UNIVERSAL SHIFT/STORAGE REGISTERS

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- Multiplexed Inputs/Outputs Provide Improved Bit Density
- Four Modes of Operations:
 

Hold (Store)	Shift Left
Shift Right	Load Data
- Operates with Outputs Enabled or at High Z
- 3-State Outputs Drive Bus Lines Directly
- Can Be Cascaded for N-Bit Word Lengths
- SN54LS323 and SN74LS323 Are Similar But Have Synchronous Clear

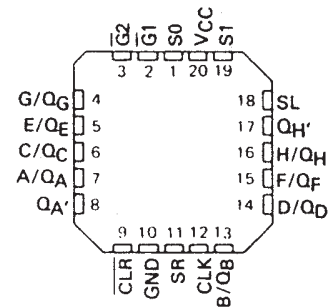
SN54LS299, SN54S299 . . . J OR W PACKAGE  
SN74LS299, SN74S299 . . . DW OR N PACKAGE  
(TOP VIEW)



- Applications:
  - Stacked or Push-Down Registers
  - Buffer Storage, and Accumulator Registers

TYPE	GUARANTEED	TYPICAL
	SHIFT (CLOCK) FREQUENCY	POWER DISSIPATION
'LS299	25 MHz	175 mW
'S299	50 MHz	700 mW

SN54LS299, SN54S299 . . . FK PACKAGE  
(TOP VIEW)



## description

These Schottky TTL eight-bit universal registers feature multiplexed inputs/outputs to achieve full eight-bit data handling in a single 20-pin package. Two function-select inputs and two output-control inputs can be used to choose the modes of operation listed in the function table.

Synchronous parallel loading is accomplished by taking both function-select lines, S0 and S1, high. This places the three-state outputs in a high-impedance state, which permits data that is applied on the input/output lines to be clocked into the register. Reading out of the register can be accomplished while the outputs are enabled in any mode. A direct overriding input is provided to clear the register whether the outputs are enabled or off.

FUNCTION TABLE

MODE	INPUTS						INPUTS/OUTPUTS								OUTPUTS			
	CLR	FUNCTION SELECT		OUTPUT CONTROL		CLK	SERIAL		A/QA	B/QB	C/QC	D/QD	E/QE	F/QF	G/QG	H/QH	QA'	QH'
		S1	S0	G1†	G2†		SL	SR										
Clear	L	X	L	L	L	X	X	X	L	L	L	L	L	L	L	L	L	L
	L	L	X	L	L	X	X	X	L	L	L	L	L	L	L	L	L	L
	L	H	H	X	X	X	X	X	X	X	X	X	X	X	X	X	X	X
Hold	H	L	L	L	L	X	X	X	QA0	QB0	QC0	QD0	QE0	QF0	QG0	QH0	QA0	QH0
	H	X	X	L	L	L	X	X	QA0	QB0	QC0	QD0	QE0	QF0	QG0	QH0	QA0	QH0
Shift Right	H	L	H	L	L	†	X	H	H	QA <sub>n</sub>	QB <sub>n</sub>	QC <sub>n</sub>	QD <sub>n</sub>	QE <sub>n</sub>	QF <sub>n</sub>	QG <sub>n</sub>	H	QH <sub>n</sub>
	H	L	H	L	L	†	X	L	L	QA <sub>n</sub>	QB <sub>n</sub>	QC <sub>n</sub>	QD <sub>n</sub>	QE <sub>n</sub>	QF <sub>n</sub>	QG <sub>n</sub>	L	QH <sub>n</sub>
Shift Left	H	H	L	L	L	†	H	X	QB <sub>n</sub>	QC <sub>n</sub>	QD <sub>n</sub>	QE <sub>n</sub>	QF <sub>n</sub>	QG <sub>n</sub>	QH <sub>n</sub>	H	QB <sub>n</sub>	H
	H	H	L	L	L	†	L	X	QB <sub>n</sub>	QC <sub>n</sub>	QD <sub>n</sub>	QE <sub>n</sub>	QF <sub>n</sub>	QG <sub>n</sub>	QH <sub>n</sub>	L	QB <sub>n</sub>	L
Load	H	H	H	X	X	†	X	X	a	b	c	d	e	f	g	h	a	h

† When one or both output controls are high the eight input/output terminals are disabled to the high-impedance state; however, sequential operation or clearing of the register is not affected.

a . . . h = the level of the steady-state input at inputs A through H, respectively. These data are loaded into the flip-flops while the flip-flop outputs are isolated from the input/output terminals.

PRODUCTION DATA information is current as of publication date. Products conform to specifications per the terms of Texas Instruments standard warranty. Production processing does not necessarily include testing of all parameters.



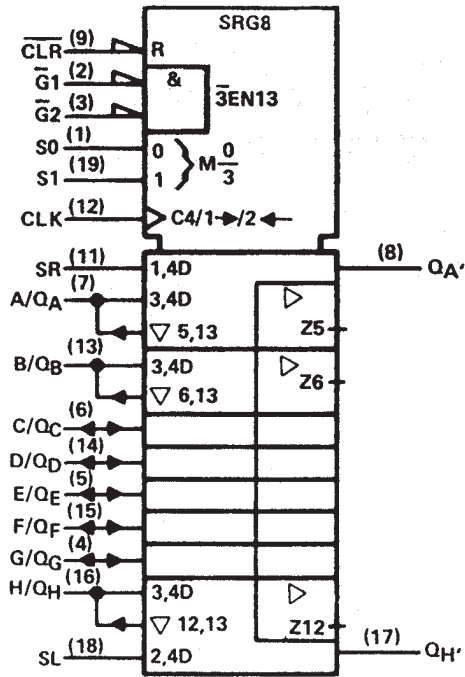
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# SN54LS299, SN54S299, SN74LS299, SN74S299 8-BIT UNIVERSAL SHIFT/STORAGE REGISTERS

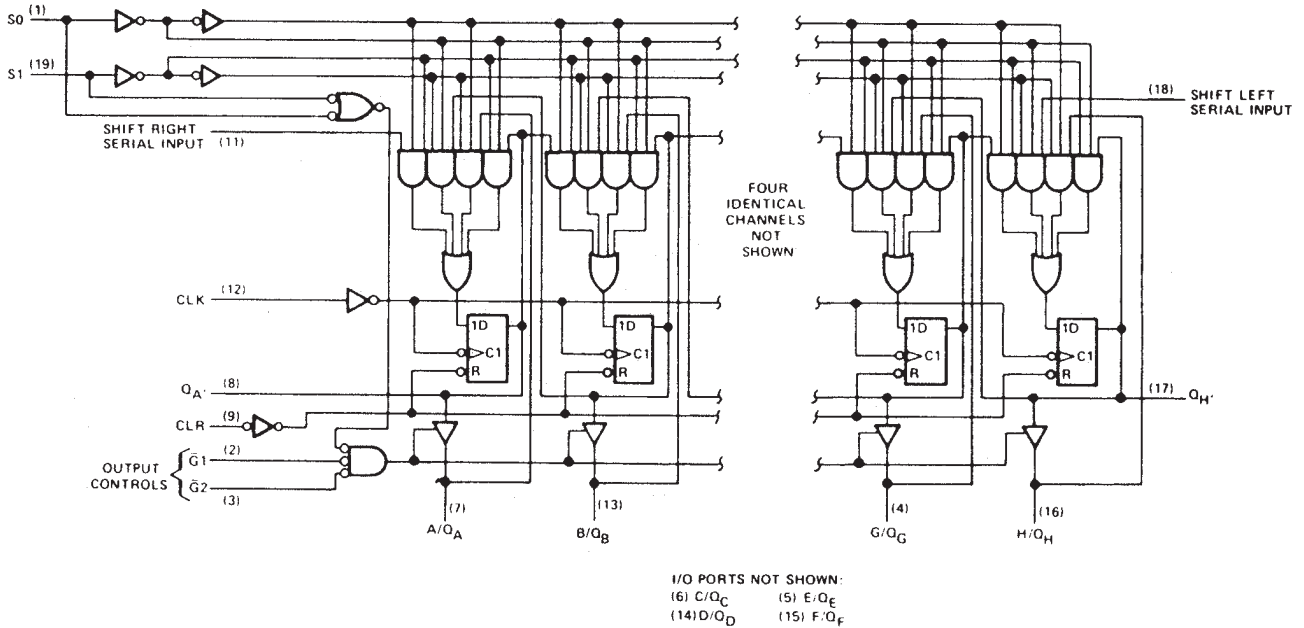
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## logic symbol†



† This symbol is in accordance with ANSI/IEEE Std 91-1984 and IEC Publication 617-12. Pin numbers shown are for DW, J, N, and W packages.

## logic diagram (positive logic)



Pin numbers shown are for DW, J, N, and W packages.

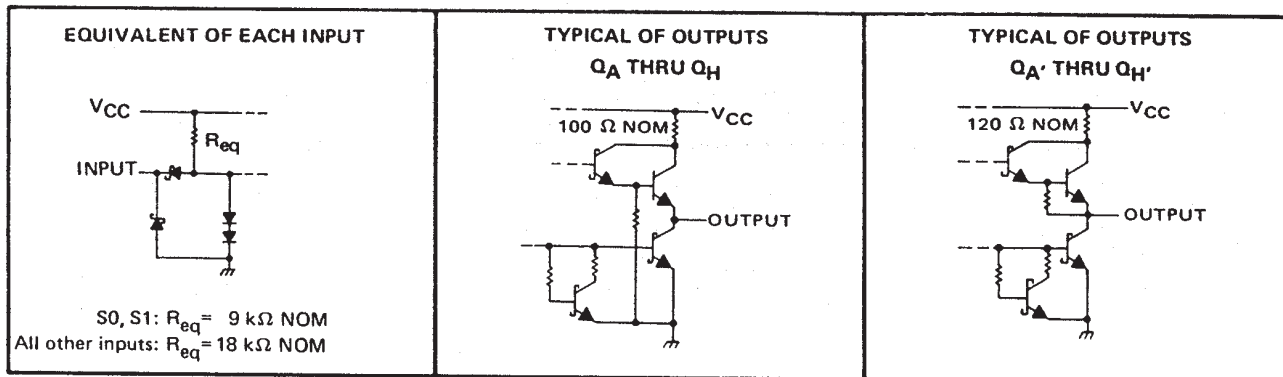


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# SN54LS299, SN54S299, SN74LS299, SN74S299 8-BIT UNIVERSAL SHIFT/STORAGE REGISTERS

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## schematics of inputs and outputs



## absolute maximum ratings over operating free-air temperature range (unless otherwise noted)

Supply voltage, $V_{CC}$ (see Note 1)	7 V
Input voltage	7 V
Off-state output voltage	5.5 V
Operating free-air temperature range: SN54LS299	$-55^{\circ}\text{C}$ to $125^{\circ}\text{C}$
SN74LS299	$0^{\circ}\text{C}$ to $70^{\circ}\text{C}$
Storage temperature	$-65^{\circ}\text{C}$ to $150^{\circ}\text{C}$

NOTE 1: Voltage values are with respect to network ground terminal.

## recommended operating conditions

		SN54LS299			SN74LS299			UNIT
		MIN	NOM	MAX	MIN	NOM	MAX	
Supply voltage, $V_{CC}$		4.5	5	5.5	4.75	5	5.25	V
High-level output current, $I_{OH}$	$Q_A$ thru $Q_H$			-1			-2.6	mA
	$Q_A'$ or $Q_H'$			-0.4			-0.4	
Low-level output current, $I_{OL}$	$Q_A$ thru $Q_H$			12			24	mA
	$Q_A'$ or $Q_H'$			4			8	
Clock frequency, $f_{clock}$		0		20	0		20	MHz
Width of clock pulse, $t_w(\text{clock})$	Clock high	30			30			ns
	Clock low	18			10			
Width of clear pulse, $t_w(\text{clear})$	Clear low	25			20			ns
	Clear high							
Setup time, $t_{su}$	Select	35 <sup>†</sup>			35 <sup>†</sup>			ns
	High-level data <sup>†</sup>	20 <sup>†</sup>			20 <sup>†</sup>			
	Low-level data <sup>†</sup>	20 <sup>†</sup>			20 <sup>†</sup>			
	Clear inactive-state	24 <sup>†</sup>			20 <sup>†</sup>			
Hold time, $t_h$	Select	10 <sup>†</sup>			10 <sup>†</sup>			ns
	Data <sup>†</sup>	3 <sup>†</sup>			0 <sup>†</sup>			
Operating free-air temperature, $T_A$		-55		125	0		70	$^{\circ}\text{C}$

<sup>†</sup> Data includes the two serial inputs and the eight input/output data lines.

# SN54LS299, SN54S299, SN74LS299, SN74S299 8-BIT UNIVERSAL SHIFT/STORAGE REGISTERS

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## electrical characteristics over recommended operating free-air temperature range (unless otherwise noted)

PARAMETER		TEST CONDITIONS†	SN54LS299		SN74LS299		UNIT			
			MIN	TYP‡	MAX	MIN		TYP‡	MAX	
V <sub>IH</sub>	High-level input voltage		2		2		V			
V <sub>IL</sub>	Low-level input voltage				0.7		0.8	V		
V <sub>IK</sub>	Input clamp voltage	V <sub>CC</sub> = MIN, I <sub>I</sub> = -18 mA			-1.5		-1.5	V		
V <sub>OH</sub>	High-level output voltage	Q <sub>A</sub> thru Q <sub>H</sub>	V <sub>CC</sub> = MIN, V <sub>IH</sub> = 2 V,		2.4	3.2	2.4	3.1	V	
		Q <sub>A</sub> ' or Q <sub>H</sub> '	V <sub>IL</sub> = V <sub>ILmax</sub> , I <sub>OH</sub> = MAX		2.5	3.4	2.7	3.4		
V <sub>OL</sub>	Low-level output voltage	Q <sub>A</sub> thru Q <sub>H</sub>	V <sub>CC</sub> = MIN, V <sub>IH</sub> = 2 V, V <sub>IL</sub> = V <sub>ILmax</sub>	I <sub>OL</sub> = 12 mA	0.25	0.4	0.25	0.4	V	
				I <sub>OL</sub> = 24 mA			0.35	0.5		
		Q <sub>A</sub> ' or Q <sub>H</sub> '		I <sub>OL</sub> = 4 mA	0.25	0.4	0.25	0.4		
				I <sub>OL</sub> = 8 mA			0.35	0.5		
I <sub>OZH</sub>	Off-state output current, high-level voltage applied	Q <sub>A</sub> thru Q <sub>H</sub>	V <sub>CC</sub> = MAX, V <sub>O</sub> = 2.7 V, V <sub>IH</sub> = 2 V,		40		40	μA		
I <sub>OZL</sub>	Off-state output current, low-level voltage applied	Q <sub>A</sub> thru Q <sub>H</sub>	V <sub>CC</sub> = MAX, V <sub>O</sub> = 0.4 V, V <sub>IH</sub> = 2 V,		-400		-400	μA		
I <sub>I</sub>	Input current at maximum input voltage	S0, S1	V <sub>CC</sub> = MAX	V <sub>I</sub> = 7 V		200		200	μA	
		A thru H		V <sub>I</sub> = 5.5 V		100		100		
		Any other		V <sub>I</sub> = 7 V		100		100		
I <sub>IH</sub>	High-level input current	A thru H, S0, S1	V <sub>CC</sub> = MAX, V <sub>I</sub> = 2.7 V			40		40	μA	
		Any other				20		20		
I <sub>IL</sub>	Low-level input current	S0, S1	V <sub>CC</sub> = MAX, V <sub>I</sub> = 0.4 V			-0.8		-0.8	mA	
		Any other				-0.4		-0.4		
I <sub>OS</sub>	Short-circuit output current§	Q <sub>A</sub> thru Q <sub>H</sub>	V <sub>CC</sub> = MAX		-30	-130	-30	-130	mA	
		Q <sub>A</sub> ' or Q <sub>H</sub> '			-20	-100	-20	-100		
I <sub>CC</sub>	Supply current		V <sub>CC</sub> = MAX		33	53		33	53	mA

† For conditions shown as MIN or MAX, use the appropriate value specified under recommended operating conditions.

‡ All typical values are at V<sub>CC</sub> = 5 V, T<sub>A</sub> = 25°C.

§ Not more than one output should be shorted at a time and duration of the short-circuit should not exceed one second.

## switching characteristics, V<sub>CC</sub> = 5 V, T<sub>A</sub> = 25°C

PARAMETER¶	FROM (INPUT)	TO (OUTPUT)	TEST CONDITIONS	MIN	TYP	MAX	UNIT
f <sub>max</sub>			See Note 2	20	35		MHz
t <sub>PLH</sub>	CLK	Q <sub>A</sub> ' or Q <sub>H</sub> '	R <sub>L</sub> = 2 kΩ, C <sub>L</sub> = 15 pF		22	33	ns
t <sub>PHL</sub>					26	39	
t <sub>PHL</sub>				CLR		27	
t <sub>PLH</sub>	CLK	Q <sub>A</sub> thru Q <sub>H</sub>	R <sub>L</sub> = 665 Ω, C <sub>L</sub> = 45 pF		17	25	ns
t <sub>PHL</sub>					26	39	
t <sub>PHL</sub>				CLR		26	
t <sub>PZH</sub>	G1, G2	Q <sub>A</sub> thru Q <sub>H</sub>			13	21	ns
t <sub>PZL</sub>					19	30	
t <sub>PHZ</sub>	G1, G2	Q <sub>A</sub> thru Q <sub>H</sub>	R <sub>L</sub> = 665 Ω, C <sub>L</sub> = 5 pF		10	20	ns
t <sub>PLZ</sub>					10	15	

¶ f<sub>max</sub> ≡ maximum clock frequency

t<sub>PLH</sub> ≡ propagation delay time, low-to-high-level output.

t<sub>PHL</sub> ≡ propagation delay time, high-to-low-level output

t<sub>PZH</sub> ≡ output enable time to high level

t<sub>PZL</sub> ≡ output enable time to low level

t<sub>PHZ</sub> ≡ output disable time from high level

t<sub>PLZ</sub> ≡ output disable time from low level

NOTE 2: For testing f<sub>max</sub>, all outputs are loaded simultaneously, each with C<sub>L</sub> and R<sub>L</sub> as specified for the propagation times.

Load circuits and voltage waveforms are shown in Section 1.

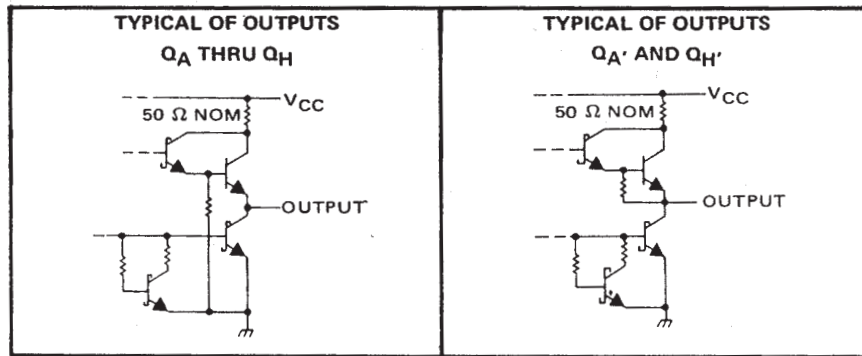
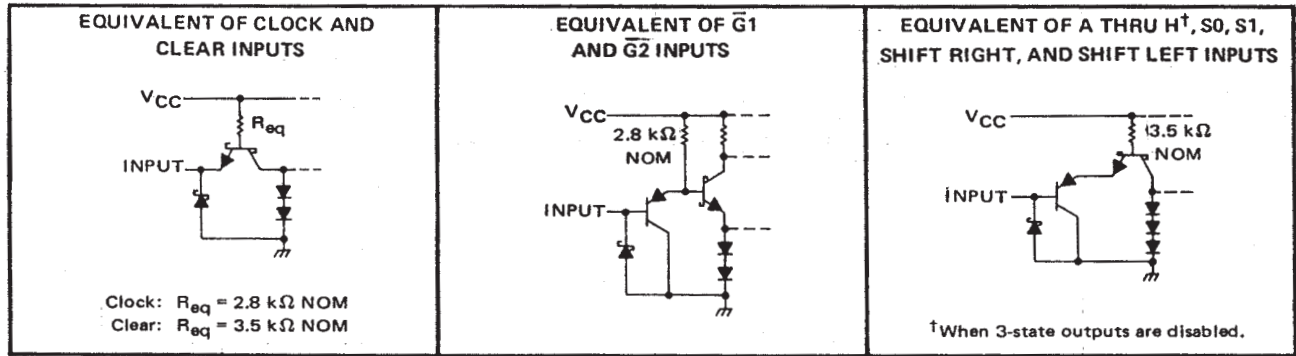


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# SN54LS299, SN54S299, SN74LS299, SN74S299 8-BIT UNIVERSAL SHIFT/STORAGE REGISTERS

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## schematics of inputs and outputs



## absolute maximum ratings over operating free-air temperature range (unless otherwise noted)

Supply voltage, $V_{CC}$ (see Note 1) .....	7 V
Input voltage .....	5.5 V
Off-state output voltage .....	5.5 V
Operating free-air temperature range: SN54S299 (See Note 1) .....	-55 °C to 125 °C
SN74S299 .....	0 °C to 70 °C
Storage temperature range .....	-65 °C to 150 °C

NOTE 1: Voltage values are with respect to network ground terminal.

## recommended operating conditions

		SN54S299			SN74S299			UNIT
		MIN	NOM	MAX	MIN	NOM	MAX	
Supply voltage, $V_{CC}$		4.5	5	5.5	4.75	5	5.25	V
High-level output current, $I_{OH}$	$Q_A$ thru $Q_H$			-2			-6.5	mA
	$Q_A'$ or $Q_H'$			-0.5			-0.5	
Low-level output current, $I_{OL}$	$Q_A$ thru $Q_H$			20			20	mA
	$Q_A'$ or $Q_H'$			6			6	
Clock frequency, $f_{clock}$		0		50	0		50	MHz
Width of clock pulse, $t_{w(clock)}$	Clock high	10			10			ns
	Clock low	10			10			
Width of clear pulse, $t_{w(clear)}$	Clear low	10			10			ns
Setup time, $t_{SU}$	Select	15 <sup>†</sup>			15 <sup>†</sup>			ns
	High-level data <sup>‡</sup>	7 <sup>†</sup>			7 <sup>†</sup>			
	Low-level data <sup>‡</sup>	5 <sup>†</sup>			5 <sup>†</sup>			
	Clear inactive-state	10 <sup>†</sup>			10 <sup>†</sup>			
Hold time, $t_H$	Select	5 <sup>†</sup>			5 <sup>†</sup>			ns
	Data <sup>‡</sup>	5 <sup>†</sup>			5 <sup>†</sup>			
Operating free-air temperature, $T_A$		-55		125	0		70	°C

<sup>†</sup> Data includes the two serial inputs and the eight input/output data lines.



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electrical characteristics over recommended operating free-air temperature range (unless otherwise noted)

PARAMETER		TEST CONDITIONS†	MIN	TYP‡	MAX	UNIT	
V <sub>IH</sub>	High-level input voltage		2			V	
V <sub>IL</sub>	Low-level input voltage				0.8	V	
V <sub>IK</sub>	Input clamp voltage	V <sub>CC</sub> = MIN, I <sub>I</sub> = -18 mA			-1.2	V	
V <sub>OH</sub>	High-level output voltage	Q <sub>A</sub> thru Q <sub>H</sub>	V <sub>CC</sub> = MIN, V <sub>IH</sub> = 2 V,	2.4	3.2	V	
		Q <sub>A</sub> ' or Q <sub>H</sub> '	V <sub>IL</sub> = 0.8 V, I <sub>OH</sub> = MAX	2.7	3.4		
V <sub>OL</sub>	Low-level output voltage	V <sub>CC</sub> = MIN, V <sub>IH</sub> = 2 V, V <sub>IL</sub> = 0.8 V, I <sub>OL</sub> = MAX			0.5	V	
I <sub>OZH</sub>	Off-state output current, high-level voltage applied	Q <sub>A</sub> thru Q <sub>H</sub>	V <sub>CC</sub> = MAX, V <sub>IH</sub> = 2 V, V <sub>O</sub> = 2.4 V		100	μA	
I <sub>OZL</sub>	Off-state output current, low-level voltage applied	Q <sub>A</sub> thru Q <sub>H</sub>	V <sub>CC</sub> = MAX, V <sub>IH</sub> = 2 V, V <sub>O</sub> = 0.5 V		-250	μA	
I <sub>I</sub>	Input current at maximum input voltage	V <sub>CC</sub> = MAX, V <sub>I</sub> = 5.5 V			1	mA	
I <sub>IH</sub>	High-level input current	A thru H, S <sub>0</sub> , S <sub>1</sub>	V <sub>CC</sub> = MAX, V <sub>I</sub> = 2.7 V		100	μA	
		Any other			50		
I <sub>IL</sub>	Low-level input current	CLK or CLR	V <sub>CC</sub> = MAX, V <sub>I</sub> = 0.5 V		-2	mA	
		S <sub>0</sub> , S <sub>1</sub>			-500	μA	
		Any other			-250	μA	
I <sub>OS</sub>	Short-circuit output current §	Q <sub>A</sub> thru Q <sub>H</sub>	V <sub>CC</sub> = MAX		-40	-100	mA
		Q <sub>A</sub> ' or Q <sub>H</sub> '			-20	-100	
I <sub>CC</sub>	Supply current	V <sub>CC</sub> = MAX		140	225	mA	

† For conditions shown as MIN or MAX, use the appropriate value specified under recommended operating conditions.

‡ All typical values are at V<sub>CC</sub> = 5 V, T<sub>A</sub> = 25°C.

§ Not more than one output should be shorted at a time and duration of the short-circuit should not exceed one second.

switching characteristics, V<sub>CC</sub> = 5 V, T<sub>A</sub> = 25°C

PARAMETER¶	FROM (INPUT)	TO (OUTPUT)	TEST CONDITIONS	MIN	TYP	MAX	UNIT
f <sub>max</sub>			See Note 2	50	70		MHz
t <sub>PLH</sub>	CLK	Q <sub>A</sub> ' or Q <sub>H</sub> '	R <sub>L</sub> = 1 kΩ, C <sub>L</sub> = 15 pF		12	20	ns
t <sub>PHL</sub>					13	20	
t <sub>PHL</sub>	CLR	Q <sub>A</sub> ' or Q <sub>H</sub> '			14	21	ns
t <sub>PLH</sub>	CLK	Q <sub>A</sub> thru Q <sub>H</sub>	R <sub>L</sub> = 280 Ω, C <sub>L</sub> = 45 pF		15	21	ns
t <sub>PHL</sub>					15	21	
t <sub>PHL</sub>	G <sub>1</sub> , G <sub>2</sub>	Q <sub>A</sub> thru Q <sub>H</sub>	R <sub>L</sub> = 280 Ω, C <sub>L</sub> = 45 pF		16	24	ns
t <sub>PZH</sub>					10	18	
t <sub>PZL</sub>	G <sub>1</sub> , G <sub>2</sub>	Q <sub>A</sub> thru Q <sub>H</sub>	R <sub>L</sub> = 280 Ω, C <sub>L</sub> = 5 pF		12	18	ns
t <sub>PHZ</sub>					7	12	
t <sub>PLZ</sub>	G <sub>1</sub> , G <sub>2</sub>	Q <sub>A</sub> thru Q <sub>H</sub>	R <sub>L</sub> = 280 Ω, C <sub>L</sub> = 5 pF		7	12	ns
t <sub>PLZ</sub>					7	12	

¶ f<sub>max</sub> = maximum clock frequency

t<sub>PLH</sub> = Propagation delay time, low-to-high-level output

t<sub>PHL</sub> = Propagation delay time, high-to-low-level output

t<sub>PZH</sub> = output enable time to high level

t<sub>PZL</sub> = output enable time to low level

t<sub>PHZ</sub> = output disable time from high level

t<sub>PLZ</sub> = output disable time from low level

NOTE 2: For testing f<sub>max</sub>, all outputs are loaded simultaneously, each with C<sub>L</sub> and R<sub>L</sub> as specified for the propagation times.

Load circuits and voltage waveforms are shown in Section 1.



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